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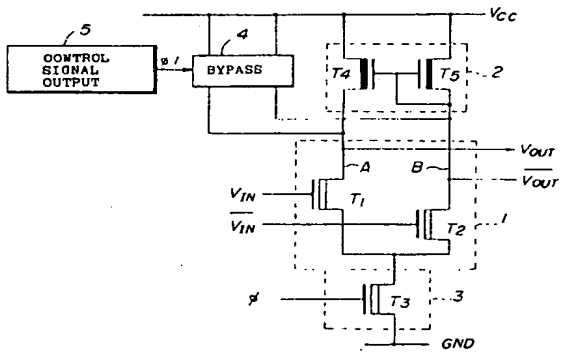
(54) **Current mirror amplifier circuit and method of driving the same.**

(57) A current mirror amplifier circuit includes a differential amplifier circuit (1) having first and second nodes (A, B) for differentially amplifying a pair of complementary input signals in an activation mode, a current mirror circuit (2) coupled between a first power source (Vcc) and the first and second nodes of the differential amplifier circuit, a switching circuit (3) coupled between the differential amplifier circuit and a second power source (GND) which supplies a second voltage lower than a first voltage supplied by the first power source for switching a mode of the differential amplifier circuit from a standby mode to the activation mode in response to an activation signal, and a circuit (4) coupled between the first power source and the first and second nodes of the differential amplifier circuit for pulling up potentials of the first and second nodes during the standby mode, where this circuit is deactivated after the differential amplifier circuit is switched from the standby mode to the activation mode.

FIG. 3



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BACKGROUND OF THE INVENTION

The present invention generally relates to current mirror amplifier circuits and methods of driving the same, and more particularly to a current mirror amplifier circuit which amplifies a signal which is read to a data bus of a semiconductor memory device or the like and a method of driving such a current mirror amplifier circuit.

There has been more demands recently to further increase the operation speeds of semiconductor devices, and the current mirror amplifier circuit is used as one means of realizing the high-speed operation. However, there is now a demand to increase the operation speed of the current mirror amplifier circuit.

Conventionally, in the current mirror amplifier circuit, it is desirable that a pair of nodes from which differentially amplified signals are obtained is set to the same level in a standby mode. If the levels of the nodes were different in the standby mode, the time it takes for the levels of the nodes to reach a threshold voltage of a circuit which is provided in a next stage becomes different depending on whether the signal level rises or falls when the operation of the current mirror amplifier circuit starts from the standby mode, thereby causing a delay in the operation of the current mirror amplifier circuit.

Accordingly, there is a proposed current mirror amplifier circuit in which the pair of nodes from which the differentially amplified signals are obtained is set to the same level in the standby mode. FIG.1 shows this proposed current mirror amplifier circuit. In FIG.1, sources of N-channel MOS transistors (hereinafter simply referred to as NMOS transistors) T1 and T2 are coupled to form a differential amplifier circuit part. The sources of the NMOS transistors T1 and T2 are coupled to ground GND via an NMOS transistor T3 which forms a switching circuit part. On the other hand, a drain of the NMOS transistor T1 is coupled to a power source Vcc via a P-channel MOS transistor (hereinafter simply referred to as a PMOS transistor) T4, and a drain of the NMOS transistor T2 is coupled to the power source Vcc via a PMOS transistor T5. Gates of the PMOS transistors T4 and T5 are connected in common to a node B which is connected to a drain of the PMOS transistor T5.

A PMOS transistor T6 is coupled in parallel to the PMOS transistor T4, and a PMOS transistor T7 is coupled in parallel to the PMOS transistor T5. An activation signal ϕ which is applied to a gate of the NMOS transistor T3 is also applied to gates of the PMOS transistors T6 and T7.

In the standby mode in which no activation signal ϕ is received by the current mirror amplifier circuit, a zero voltage is applied to the gates of the PMOS transistors T6 and T7 and the NMOS transistor T3. Accordingly, the NMOS transistor T3 is OFF and the PMOS transistors T6 and T7 are ON. In addition, the potentials at the nodes A and B from which output signals V_{OUT} and $\overline{V}_{OUT}$ are respectively obtained are set to the same level, that is, the power source voltage Vcc.

When the activation signal ϕ is received in this state, the power source voltage Vcc is applied to the gates of the PMOS transistors T6 and T7 and the NMOS transistor T3. Hence, the PMOS transistors T6 and T7 turn OFF and the NMOS transistor T3 turns ON. As a result, the potentials at the nodes A and B both begin to fall. The PMOS transistors T4 and T5 turn ON when the potential at the node B falls to a level which is a threshold voltage Vth of the PMOS transistor T5 lower than the power source voltage Vcc.

If a signal V_{IN} applied to a gate of the NMOS transistor T1 is lower than a signal $\overline{V}_{IN}$ which is applied to a gate of the NMOS transistor T2, the potential at the node A increases towards the high potential side while the potential at the node B decreases towards the low potential side, as shown in FIG.2. In other words, the potentials at the nodes A and B are differentially amplified.

Because the potentials at the nodes A and B of the current mirror amplifier circuit shown in FIG.1 are set to the same level in the standby mode, the rise and fall times of the output signals V_{OUT} and $\overline{V}_{OUT}$ output via the nodes A and B required to reach the threshold voltage of the circuit provided in the next stage are constant when the operation of the current mirror amplifier circuit is started from the standby mode. In other words, the time it takes for the potentials at the nodes A and B to reach the threshold voltage of the circuit which is provided in the next stage becomes constant, thereby preventing a delay in the operation of the current mirror amplifier circuit.

In addition, according to the current mirror amplifier circuit shown in FIG.1, the PMOS transistors T6 and T7 are ON in the standby mode and the potentials at the nodes A and B are set to the same power source voltage Vcc. For this reason, the potentials at the nodes A and B will not become higher than the power source voltage Vcc even if the power source voltage Vcc fluctuates due to noise or the like and the nodes A and B assume floating states. Further, since a symmetrical circuit construction is realized by coupling the PMOS transistors T6 and T6 in parallel with the corresponding PMOS transistors T4 and T5, the pattern design of the current mirror amplifier circuit is facilitated and a fine electrical characteristic is obtained.

However, when the current mirror amplifier cir-

cuit shown in FIG.1 receives the activation signal ϕ, no current path exists from the power source Vcc to the ground GND because the PMOS transistors T6 and T7 turn OFF. In other words, the potentials at the nodes A and B fall by discharge. But when the potential fall at the node B to a voltage which is the threshold voltage Vth lower than the power source voltage Vcc for the purpose of turning ON the PMOS transistors T4 and T5 depends on the discharge, the potential fall takes time and there is a problem in that the operation speed of the current mirror amplifier circuit cannot be further improved.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a novel and useful current mirror amplifier circuit and method of driving the current mirror amplifier circuit, in which the problem described above is eliminated.

Another and more specific object of the present invention is to provide a current mirror amplifier circuit comprising differential amplifier circuit means, having first and second nodes, for differentially amplifying a pair of complementary input signals in an activation mode, current mirror circuit means coupled between a first power source and the first and second nodes of said differential amplifier circuit means, switching circuit means, coupled between said differential amplifier circuit means and a second power source which supplies a second voltage lower than a first voltage supplied by the first power source, for switching a mode of said differential amplifier circuit means from a standby mode to the activation mode in response to an activation signal, and first circuit means, coupled between the first power source and the first and second nodes of said differential amplifier circuit means, for pulling up potentials of the first and second nodes during the standby mode, where the first circuit means is deactivated after the differential amplifier circuit means is switched from the standby mode to the activation mode. According to the current mirror amplifier circuit of the present invention, it is possible to realize a high-speed operation.

Still another object of the present invention is to provide a current mirror amplifier circuit of the above type wherein the control signal is delayed by a predetermined time relative to the activation signal.

A further object of the present invention is to provide a method of driving a current mirror amplifier circuit which comprises differential amplifier circuit means, having first and second nodes, for differentially amplifying a pair of complementary input signals in an activation mode, current mirror circuit means coupled between a first power source and the first and second nodes of said differential amplifier circuit means, switching circuit means, coupled between said differential amplifier circuit means and a second power source which supplies a second voltage lower than a first voltage supplied by the first power source, for switching a mode of said differential amplifier circuit means from a standby mode to the activation mode when activated in response to an activation signal, and first circuit means, coupled between the first power source and the first and second nodes of said differential amplifier circuit means, for pulling up potentials of the first and second nodes during the standby mode, where said method comprises the steps of supplying the complementary input signals to said differential amplifier circuit means and the activation signal to said switching circuit means, and supplying the control signal to said first circuit means after a predetermined time elapses from a time when said switching circuit means is activated by the activation signal. According to the method of driving the current mirror amplifier circuit of the present invention, it is possible to realize a high-speed operation.

Other objects and further objects of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a circuit diagram showing an example of a proposed current mirror amplifier circuit;

FIG.2 shows output signal waveforms of the current mirror amplifier circuit shown in FIG.1;

FIG.3 is a circuit diagram for explaining an operating principle of a current mirror amplifier circuit according to the present invention;

FIG.4 is a circuit diagram showing an embodiment of the current mirror amplifier circuit according to the present invention;

FIG.5 shows output signal waveforms of the embodiment shown in FIG.4;

FIG.6 is a circuit diagram showing an application of the embodiment;

FIGS.7A and 7B show signal waveforms at various parts of the circuit shown in FIG.6 for explaining the effects of the embodiment;

FIG.8 is a system block diagram showing an example of a semiconductor memory device; and

FIG.9 is a circuit diagram showing the application of the current mirror amplifier circuit according to the present invention to the semiconductor memory device shown in FIG.8.

DESCRIPTION OF THE PREFERRED EMBODI-

MENTS

First, a description will be given of an operating principle of a current mirror amplifier circuit according to the present invention, by referring to FIG.3. The current mirror amplifier circuit shown in FIG.3 includes a differential amplifier circuit part 1, a current mirror circuit part 2, a switching circuit part 3, a bypass circuit part 4 and a control signal output circuit part 5 which are coupled as shown.

The differential amplifier circuit part 1 includes first and second transistors T1 and T2 which respectively receive input signals V_{IN} and $\overline{V}_{IN}$. The load side of the differential amplifier circuit part 1 is coupled to a power source Vcc via the current mirror circuit part 2. This current mirror circuit part 2 includes third and fourth transistors T3 and T4. On the other hand, the low voltage side of the differential amplifier circuit part 1 is coupled to a power source GND via the switching circuit part 3. The power source Vcc supplies a power source voltage Vcc which is higher than a voltage supplied by the power source GND. The switching circuit part 3 includes a transistor T3 which is responsive to an activation signal ϕ, and the mode of the differential amplifier circuit part 1 is changed from a standby mode to an activation mode based on the activation signal ϕ. For example, the power source Vcc supplies a voltage of 5 V, and the power source GND supplies a ground voltage which is 0 V.

The bypass circuit part 4 is coupled in parallel to the current mirror circuit part 2, and bypasses the differential amplifier circuit part 1 to the power source Vcc when activated. The control signal output circuit part 5 supplies a control signal $\phi 1$ to the bypass circuit part 5 and controls the bypass circuit part 5 to the inactive state from the active state after the current mirror amplifier circuit receives the activation signal ϕ.

In the standby mode, the bypass circuit part 4 bypasses the differential amplifier circuit part 1 to the power source Vcc in response to the control signal $\phi 1$ which is received from the control signal output circuit part 5. In this state, the potentials at two nodes A and B from which output signal V_{OUT} and $\overline{V}_{OUT}$ are obtained are set to the same power source voltage Vcc.

When the current mirror amplifier circuit receives the activation signal ϕ and the transistor T3 of the switching circuit part 3 turns ON, a current path is formed between the power source Vcc and the power source GND even though the transistors T4 and T5 within the current mirror circuit part 2 are not yet ON, because the bypass circuit part 4 still bypasses the differential amplifier circuit part 1 to the power source Vcc. As a result, the differential amplifier circuit part 1 quickly starts the operation of differentially amplifying the input signals V_{IN} and $\overline{V}_{IN}$ based on the current which flows through the bypass circuit part 4.

When the transistors T4 and T5 within the current mirror circuit part 2 eventually turn ON, the bypass circuit part 4 stops bypassing the differential amplifier circuit part 1 to the power source Vcc in response to the control signal $\phi 1$ which is received from the control signal output circuit part 5.

Next, a description will be given of an embodiment of the current mirror amplifier circuit according to the present invention, by referring to FIG.4. In this embodiment, the present invention is applied to the type of current mirror amplifier circuit shown in FIG.1. In FIG.4, those parts which are the same as those corresponding parts in FIG.1 are designated by the same reference numerals, and a description thereof will be omitted.

In FIG.4, PMOS transistors T11 and T12 form a bypass circuit part. The PMOS transistor T11 is coupled in parallel to the PMOS transistor T4 of the current mirror circuit part, and the PMOS transistor T12 is coupled in parallel to the PMOS transistor T5 of the current mirror circuit part. A control signal $\phi 1$ which is output from a control signal output circuit part is applied to gates of the PMOS transistors T11 and T12.

The control signal output circuit part includes inverter circuits INV1 and INV2, a resistor R1 and a capacitor C which are coupled as shown. The activation signal ϕ which is applied to the gate of the NMOS transistor T3 of a switching circuit part is also applied to the inverter circuit INV1 which is provided in a first stage of the control signal output circuit part. The resistor R1 and the capacitor C form a delay circuit which delays the activation signal ϕ by a delay time t which is determined by circuit constants of the delay circuit. The delayed activation signal ϕ is inverted by the inverter circuit INV2 and is formed into the control signal $\phi 1$ which is applied to the gates of the PMOS transistors T11 and T12. The delay time t is preset. In this embodiment, the delay time t is set to the time it takes for the PMOS transistor T5 of the current mirror circuit part to turn ON from a time when the NMOS transistor T3 turns ON in response to the activation signal ϕ in a state where the PMOS transistors T11 and T12 are ON, that is, the time it takes for the potential at the node B to fall from the power source voltage Vcc to a voltage which is a threshold voltage Vth of the PMOS transistor T5 lower than the power source voltage Vcc.

Next, a description will be given of the operation of this embodiment.

When the activation signal ϕ and the control signal $\phi 1$ are zero volt and the current mirror circuit part is in the standby mode, the transistors T1 through T5 are OFF. On the other hand, the

PMOS transistors T11 and T12 are ON. Accordingly, the nodes A and B from which the output signals V_{OUT} and $\overline{V}_{OUT}$ are respectively obtained are directly connected to the same power source Vcc, and thus, the potentials at the nodes A and B become the same power source voltage Vcc. As a result, since the potentials at the nodes A and B are always set to the same level in the standby mode, the time it takes for the potentials at the nodes A and B to rise and fall always becomes constant.

Next, when the current mirror amplifier circuit receives the activation signal ϕ having the power source voltage Vcc, the NMOS transistor T3 turns ON immediately responsive thereto. On the other hand, by the provision of the delay circuit which is made up of the resistor R1 and the capacitor C, the control signal $\phi 1$ does not immediately become the power source voltage Vcc but remains at zero volt. Hence, the PMOS transistors T11 and T12 remain ON. For this reason, a current path is formed between the power source Vcc and the ground GND so that a current can flow from the power source Vcc to the ground GND, and the NMOS transistors T1 and T2 of the differential amplifier circuit part quickly starts the operation of differentially amplifying the input signals V_{IN} and $\overline{V}_{IN}$. In other words, when the input signal V_{IN} is lower than the input signal $\overline{V}_{IN}$, the potential at the node A will not fall greatly once together with the potential at the node B, and the potential at the node A undergoes a change different from the potential at the node B at an early stage. Thus, the actual amplifying operation is started quickly. Therefore, even when the PMOS transistors T4 and T5 of the current mirror circuit are OFF, the NMOS transistors T1 and T2 quickly start the operation of differentially amplifying the input signals V_{IN} and $\overline{V}_{IN}$.

When the potential at the node B becomes a voltage which is the threshold voltage Vth lower than the power source voltage Vcc, the PMOS transistors T4 and T5 of the current mirror circuit part turn ON. In this state, the control signal $\phi 1$ becomes the power source voltage Vcc, and the PMOS transistors T11 and T12 turn OFF. Hence, the NMOS transistors T1 and T2 thereafter differentially amplify the input signals V_{IN} and $\overline{V}_{IN}$ based on the current which is received from the current mirror circuit part.

Therefore, according to this embodiment, a current path is formed via the PMOS transistors T11 and T12 to put the NMOS transistors T1 and T2 of the differential amplifier circuit part in the active state from the time when the activation signal ϕ is received by the current mirror amplifier circuit until the time when the current mirror circuit part becomes active. For this reason, the operation speed of the current mirror amplifier circuit can be improved.

Next, a description will be given of an application of this embodiment so as to facilitate the understanding of the effects obtainable thereby. In this application, a circuit which is provided in a stage next to the current mirror amplifier circuit is also a current mirror amplifier circuit of the same type, as shown in FIG.6. In FIG.6, those parts which are the same as those corresponding parts in FIG.4 are designated by the same reference numerals, and a description thereof will be omitted.

In this case, the potentials at the nodes A and B change as shown in FIG.7A, similarly as in the case shown in FIG.5. It is assumed that the input signal V_{IN} is a low-level signal, and the input signal $\overline{V}_{IN}$ is a high-level signal. In addition, the potentials at nodes C, D, E and F change as shown in FIG.7A, where VTH denotes a threshold voltage of inverters INV3 and INV4. As may be seen from FIG.7A, the amplification in the circuit provided in the second stage starts early because the differential amplification of the potentials at the nodes A and B of the circuit provided in the first stage occurs quickly.

On the other hand, when the current mirror amplifier circuit shown in FIG.1 is connected in two stages similarly to the circuit shown in FIG.6, the potentials at the corresponding nodes A, B, C, D, E and F become as shown in FIG.7B. From a comparison of FIGS.7A and 7B, it is readily seen that the data propagation becomes Δt faster in this application when compared to the corresponding circuit realized by use of the current mirror amplifier circuit shown in FIG.1.

The timing of the control signal $\phi 1$ should be delayed compared to that of the activation signal ϕ. Preferably, the control signal $\phi 1$ is generated at the timing when the potential at the node B becomes the threshold voltage Vth lower than the power source voltage Vcc. On the other hand, the effect of improving the operation speed of the current mirror amplifier circuit fades when the control signal $\phi 1$ is generated after the potentials at the nodes A and B saturate.

Semiconductor memory devices generally have a memory cell array in which a number of memory cell transistors are arranged in rows and columns. In correspondence to each memory cell transistor, there is provided a memory cell capacitor for storing binary data in the form of electric charges. The memory cell transistors are connected to word lines extending in a row direction and bit lines extending in a column direction, and addressing of the memory cell is made by selecting one of the word lines and one of the bit lines.

When writing data, the data to be written is supplied to a bit line and transferred to a selected memory cell capacitor via a memory cell transistor

by energizing a selected word line simultaneously. When reading data, on the other hand, the electric charges accumulated in a memory cell capacitor are transferred to a selected bit line via a memory cell transistor by energizing a selected word line. The minute change of voltage level thus induced on the bit line is detected and amplified by a sense amplifier.

In such semiconductor memory devices, various efforts are made to increase the speed of reading and writing. Among others, there is a technique to increase the speed of reading by amplifying the electric signals obtained on the bit line after amplification by a sense amplifier.

FIG.8 shows an example of a semiconductor memory device which employs the foregoing construction for increasing the speed of reading.

Referring to FIG.8, the semiconductor memory device includes a memory cell array 11 in which a number of memory cells 11a are arranged in rows and columns. Each memory cell 11a is connected to a pair of complementary bit lines BL and $\overline{BL}$ and a word line WL, wherein the bit lines are selectively enabled by a row decoder 14. The word lines, on the other hand, are enabled by a column decoder 13. Further, the column decoder 13 and the row decoder 14 are driven by an address buffer 15 which supplies a column selection signal to the row decoder 14 in response to address data ADDRESS supplied thereto.

To write data to the memory cell 11a in the memory cell array 11, an input buffer circuit 17 is used. The input buffer circuit 17 is supplied with input data Din and supplies the same to a pair of complementary data bus lines DB and $\overline{DB}$ in the form of complementary electric signals. The data bus lines DB and $\overline{DB}$ are connected to the bit lines BL and $\overline{BL}$ via an input/output gate 12. The column decoder 13 controls the input/output gate 12 in response to the column selection signal supplied thereto, and the complementary electric signals on the data bus lines DB and $\overline{DB}$ are transferred to the selected pair of bit lines BL and $\overline{BL}$. Thereby, the electric signals on the data bus lines DB and $\overline{DB}$ are transferred to the selected pair of bit lines BL and $\overline{BL}$. Further, by selectively energizing the word line WL simultaneously, the electric signals on the selected pair of bit lines BL and $\overline{BL}$ are transferred to the memory cell 11a and stored therein in the form of electric charges.

When reading data, the row decoder 14 energizes a selected word line WL. Thereby, the memory cells 11a connected to the selected word line WL transfer the electric charges stored therein to the respective pairs of bit lines BL and $\overline{BL}$, and the minute voltage change caused in the bit lines is detected by a sense amplifier SA within the input/output gate 12. The sense amplifier SA supplies the output thereof to the pair of bit lines BL and $\overline{BL}$, and the electric voltages thus produced on a selected bit line pair are supplied to the complementary data bus lines DB and $\overline{DB}$ via the input/output gate 12. The voltage signals thus obtained on the data bus lines DB and $\overline{DB}$ are then output by an output buffer circuit 16 as output data Dout.

In order to accelerate the reading, there is provided a current mirror amplifier 22 between the data bus lines DB and $\overline{DB}$ and the output buffer circuit 16 for amplifying the electric signals on the data bus lines DB and $\overline{DB}$. By amplifying the level of the complementary signals on the data bus lines DB and $\overline{DB}$, the current mirror amplifier 22 enables a quick discrimination of the logic state of the data read from the memory cell 11a.

FIG.9 shows the application of the current mirror amplifier circuit according to the present invention to the semiconductor memory device shown in FIG.8. In FIG.9, those parts which are the same as those corresponding parts in FIG.6 are designated by the same reference numerals, and a description thereof will be omitted.

Referring to FIG.9, the sense amplifier SA is provided in correspondence with each pair of bit lines BL and $\overline{BL}$. Further, the bit lines BL and $\overline{BL}$ are connected respectively to the data bus lines DB and $\overline{DB}$ via transistors 12a and 12b which form the input/output gate 12. The transistors 12a and 12b are turned ON in response to the high-level state of a column selection signal ϕ_A and connects the bit lines BL and $\overline{BL}$ to the corresponding data bus lines DB and $\overline{DB}$.

The electric signals thus transferred to the data bus lines DB and $\overline{DB}$ are then passed through a limiter circuit 23. The limiter circuit 23 includes a first transistor Tr1 connected between the power source line Vcc and the bit line BL, and a second transistor Tr2 connected between the power source line Vcc and the bit line $\overline{BL}$. Each of the transistors Tr1 and Tr2 has a gate and a source connected with each other and is maintained always at the turned-ON state. Thereby, a voltage drop corresponding to the threshold voltage of the transistors Tr1 and Tr2 appears at the drain of these transistors, and the voltage of the data bus lines DB and $\overline{DB}$ is held at the level of Vcc-VthN, where VthN represents the threshold voltage of the transistors Tr1 and Tr2. For example, the voltage level of the data bus line may be held at 4 V, assuming that the power source voltage Vcc is 5 V and the threshold voltage VthN is 1 V.

When there occurs a transfer of the electric signals from the bit lines BL and $\overline{BL}$ to the data bus lines DB and $\overline{DB}$ in response to the high-level state of the column selection signal ϕ_A, the voltage level of the data bus lines DB and $\overline{DB}$ changes about the

foregoing level of 4 V, and thus voltage change is detected by the current mirror amplifier 22.

The current mirror amplifier 22 includes two current mirror amplifier circuits 22a and 22b having a similar construction. The construction of this current mirror amplifier 22 is basically the same as that shown in FIG.6, and a description thereof will be omitted.

The present invention is not limited to the embodiment described above, and the present invention may be applied to a current mirror amplifier circuit which is formed by bipolar transistors, for example. In addition, the control signal output circuit part may include an even number of inverter circuits coupled in series so that the the control signal $\phi 1$ is produced by setting the delay time based on the number of inverter circuits. Moreover, the control signal $\phi 1$ does not necessarily have to be a signal which is produced within the current mirror amplifier circuit, and may be an external signal which is generated by a circuit or device provided externally to the current mirror amplifier circuit.

Further, the present invention is not limited to these embodiments, but various variations and modifications may be made without departing from the scope of the present invention.

Claims

1. A current mirror amplifier circuit for generating a pair of complementary output signals comprising: differential amplifier circuit means (1), having first and second nodes (A, B), for differentially amplifying a pair of complementary input signals in an activation mode; current mirror circuit means (2) coupled between a first power source (Vcc) and the first and second nodes of said differential amplifier circuit means; and switching circuit means (3), coupled between said differential amplifier circuit means and a second power source (GND) which supplies a second voltage lower than a first voltage supplied by the first power source, for switching a mode of said differential amplifier circuit means from a standby mode to the activation mode in response to an activation signal, characterized in that there is provided: first circuit means (4), coupled between the first power source (Vcc) and the first and second nodes (A, B) of said differential amplifier circuit means (1), for pulling up potentials of the first and second nodes (A, B) during the standby mode, said first circuit means being deactivated after the differential amplifier circuit means (1) is switched from the standby mode to the activation mode.

2. The current mirror amplifier circuit as claimed in claim 1, characterized in that the control signal is delayed by a predetermined time relative to the activation signal.

3. The current mirror amplifier circuit as claimed in claim 1 or 2, characterized in that there is further provided control signal output circuit means (5) for generating the control signal based on the activation signal and for supplying the control signal to said first circuit means (4).

4. The current mirror amplifier circuit as claimed in claim 1, characterized in that said differential amplifier circuit means (1) includes:

a first transistor (T1) having a gate which receives one of the complementary input signals and a drain which is connected to the first node (A), and a second transistor (T2) having a gate which receives the other of the complementary input signals and a drain which is connected to the second node (B), sources of the first and second transistors being coupled in common to said switching circuit means (3),

said current mirror circuit means (2) includes:

a third transistor (T4) having a source which is coupled to the first power source (Vcc) and a drain which is coupled to the first node (A), and a fourth transistor (T5) having a source which is coupled to the first power source and a drain which is coupled to the second node (B), gates of the third and fourth transistors being coupled in common to the second node, and

said switching circuit means (3) includes:

a fifth transistor (T3) having a gate which receives the activation signal and a source and a drain which are respectively coupled to the second power source (GND) and the sources of the first and second transistors within said differential amplifier circuit means.

5. The current mirror amplifier circuit as claimed in claim 4, characterized in that said current mirror circuit means (2) includes a sixth transistor (T6) which is coupled in parallel to the third transistor (T4), and a seventh transistor (T7) which is coupled in parallel to the fourth transistor (T5).

6. The current mirror amplifier circuit as claimed in claim 4 or 5, characterized in that the first, second and fifth transistors (T1, T2, T3) are N-channel MOS transistors, the third and fourth transistors (T4, T5) are P-channel MOS transistors, the first voltage is a positive voltage and

the second voltage is a ground voltage.

7. The current mirror amplifier circuit as claimed in any of claims 4 to 6, characterized in that the control signal is delayed by a predetermined time relative to the activation signal.

8. The current mirror amplifier circuit as claimed in claim 7, characterized in that the control signal is generated at a time when a potential at the second node (B) becomes a threshold voltage of the fourth transistor (T5) lower than the first voltage.

9. The current mirror amplifier circuit as claimed in any of claims 4 to 8, characterized in that there is further provided control signal output circuit means (5) for generating the control signal based on the activation signal and for supplying the control signal to said first circuit means (4), said control signal output circuit means including a delay circuit (R1, C) for generating the control signal by delaying the activation signal by a predetermined time so that the control signal is generated before potentials at the first and second nodes (A, B) saturate.

10. A method of driving a current mirror amplifier circuit which comprises differential amplifier circuit means (1), having first and second nodes (A, B), for differentially amplifying a pair of complementary input signals in an activation mode; current mirror circuit means (2) coupled between a first power source (Vcc) and the first and second nodes of said differential amplifier circuit means; switching circuit means (3), coupled between said differential amplifier circuit means and a second power source (GND) which supplies a second voltage lower than a first voltage supplied by the first power source, for switching a mode of said differential amplifier circuit means from a standby mode to the activation mode when activated in response to an activation signal; and first circuit means (4), coupled between the first power source and the first and second nodes of said differential amplifier circuit means, for pulling up potentials of the first and second nodes (A, B) during the standby mode, characterized in that said method comprises the steps of:

(a) supplying the complementary input signals to said differential amplifier circuit means (1) and the activation signal to said switching circuit means (3); and

(b) supplying the control signal to said first circuit means (4) after a predetermined time elapses from a time when said switching circuit means (3) is activated by the activation signal.

11. The method of driving the current mirror amplifier circuit as claimed in claim 10, characterized in that said current mirror circuit means (2) includes a first transistor (T4) having a source which is coupled to the first power source (Vcc) and a drain which is coupled to the first node (A), and a second transistor (T5) having a source which is coupled to the first power source and a drain which is coupled to the second node (B), gates of the first and second transistors being coupled in common to the second node, and said step (b) supplies to said first circuit means (4) the control signal at a time when a potential at the second node (B) becomes a threshold voltage of the second transistor (T5) lower than the first voltage.

12. The method of driving the current mirror amplifier circuit as claimed in claim 10 or 11, characterized in that said step (b) generates the control signal by delaying the activation signal by a predetermined time so that the control signal is generated before potentials at the first and second nodes (A, B) saturate.

FIG. 1 PRIOR ART

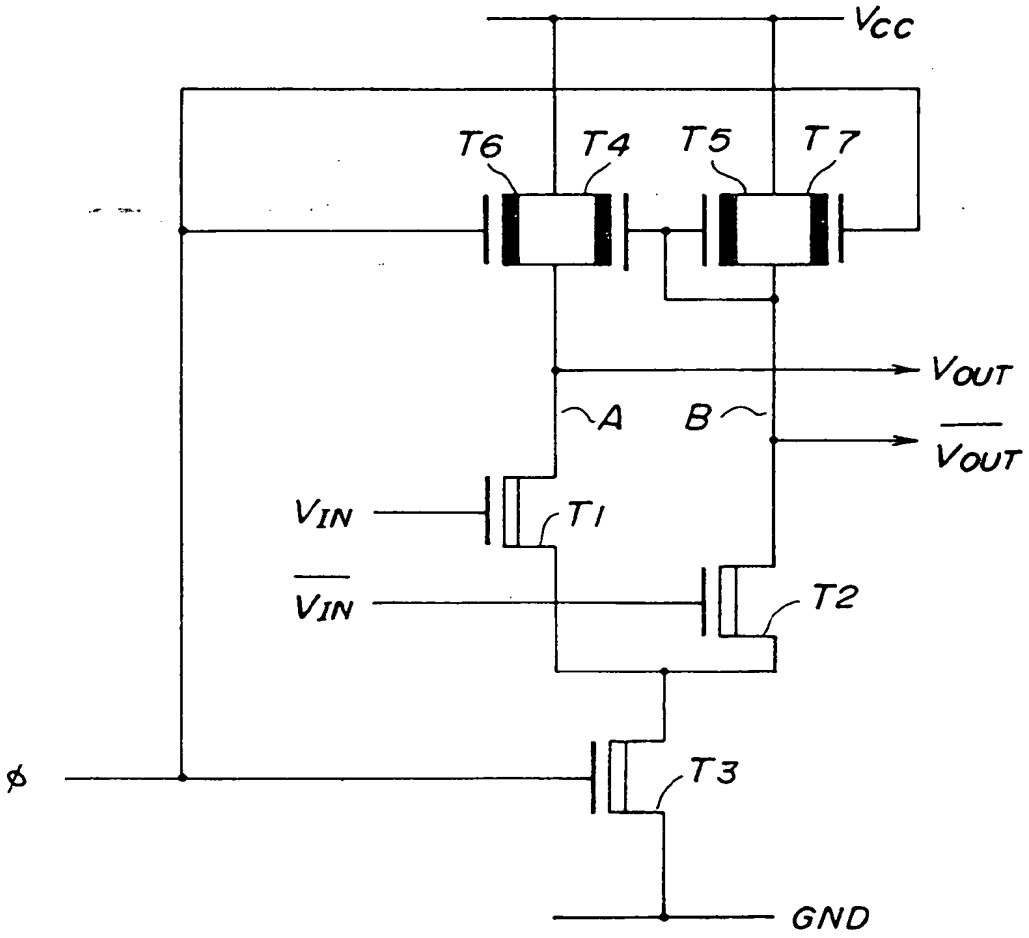


FIG.2 PRIOR ART

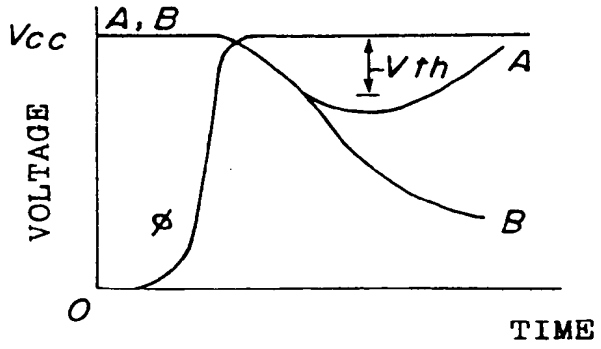


FIG.5

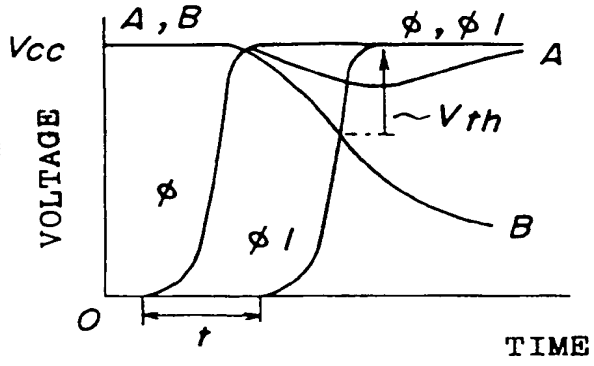


FIG. 3

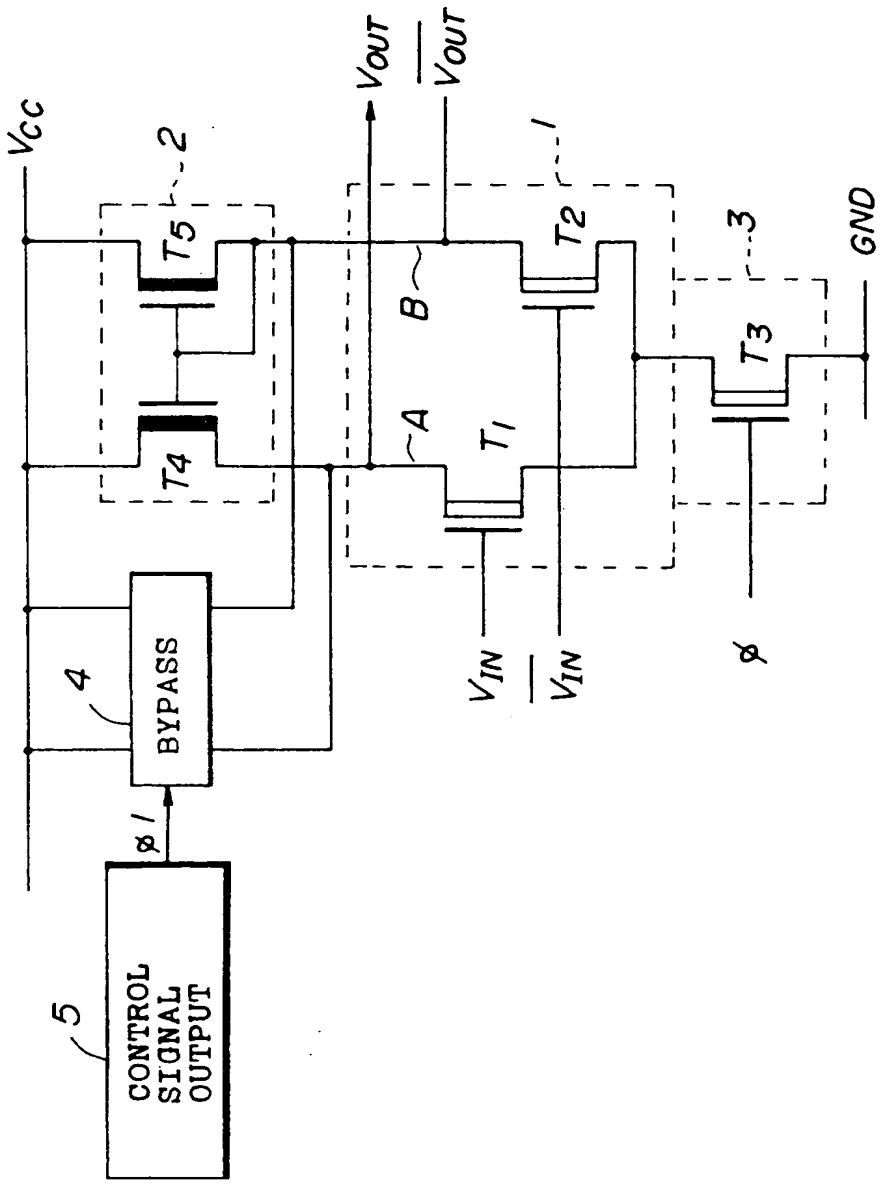


FIG.4

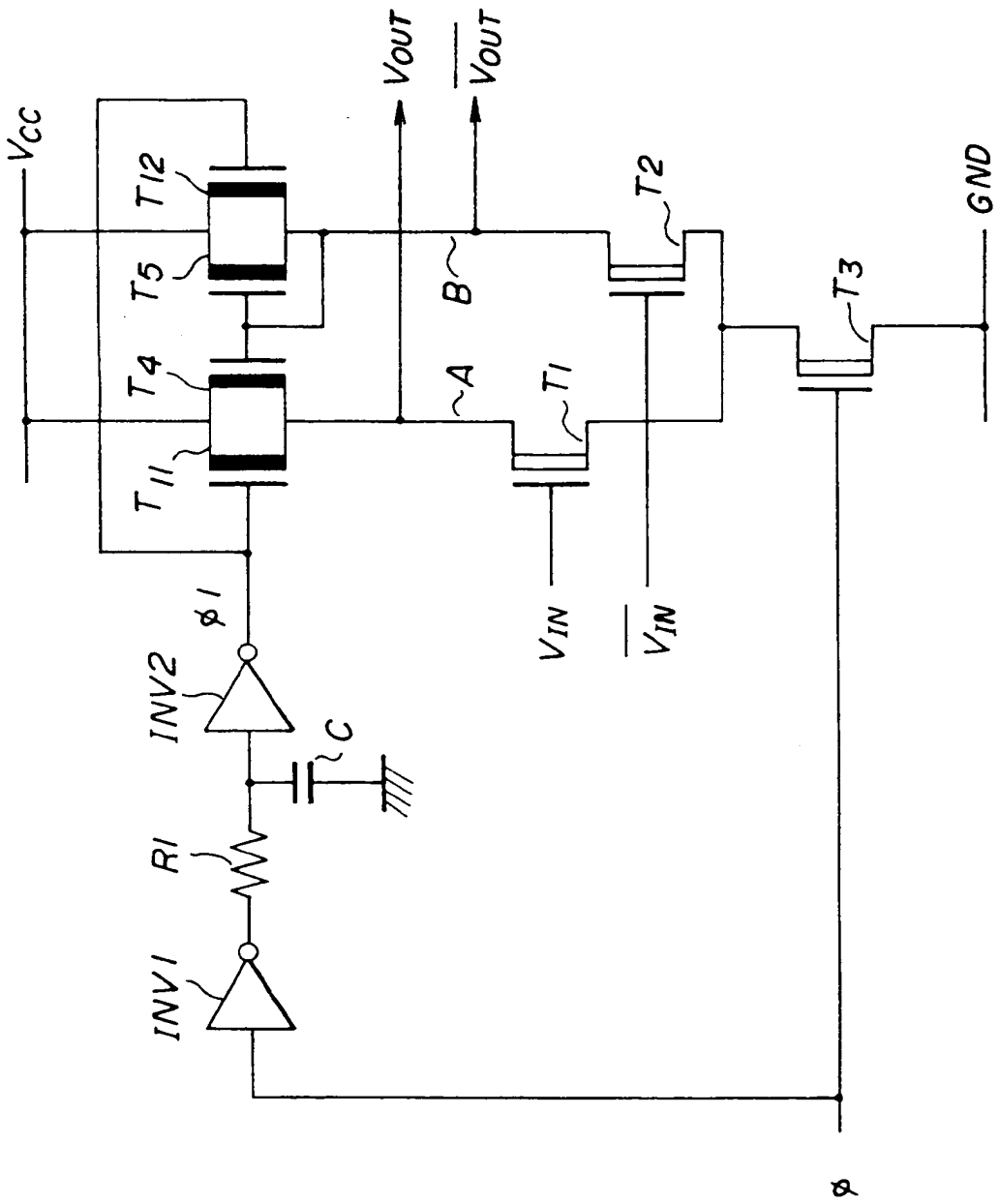
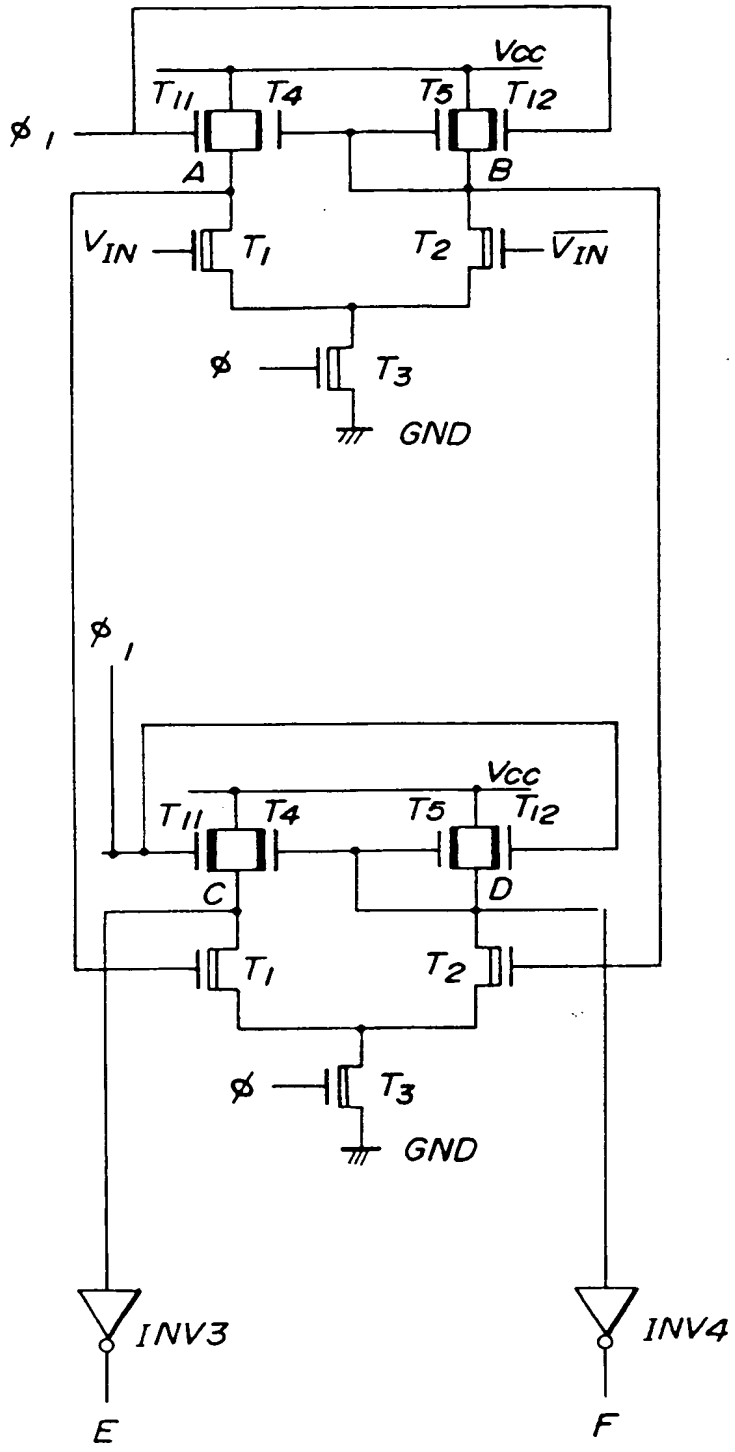

VCC
T12
T5
T4
T11
VOUT
VOUT
B
A
T2
T1
T3
GND
VIN
VIN
φ1
INV2
C
R1
INV1
φ

FIG. 6



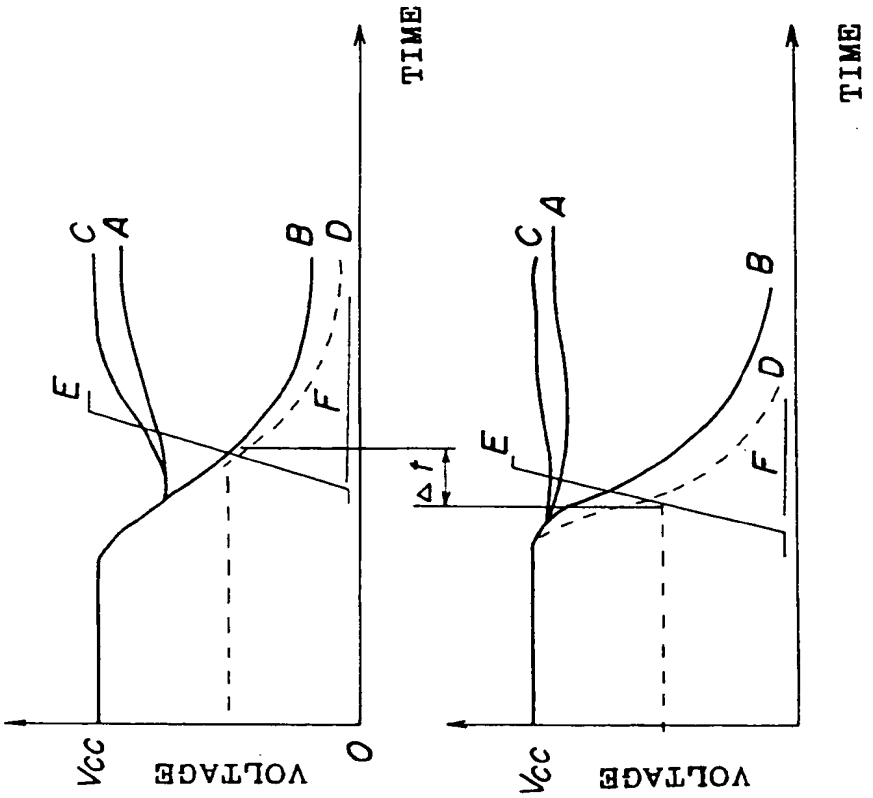


FIG.7A

FIG.7B

FIG.8

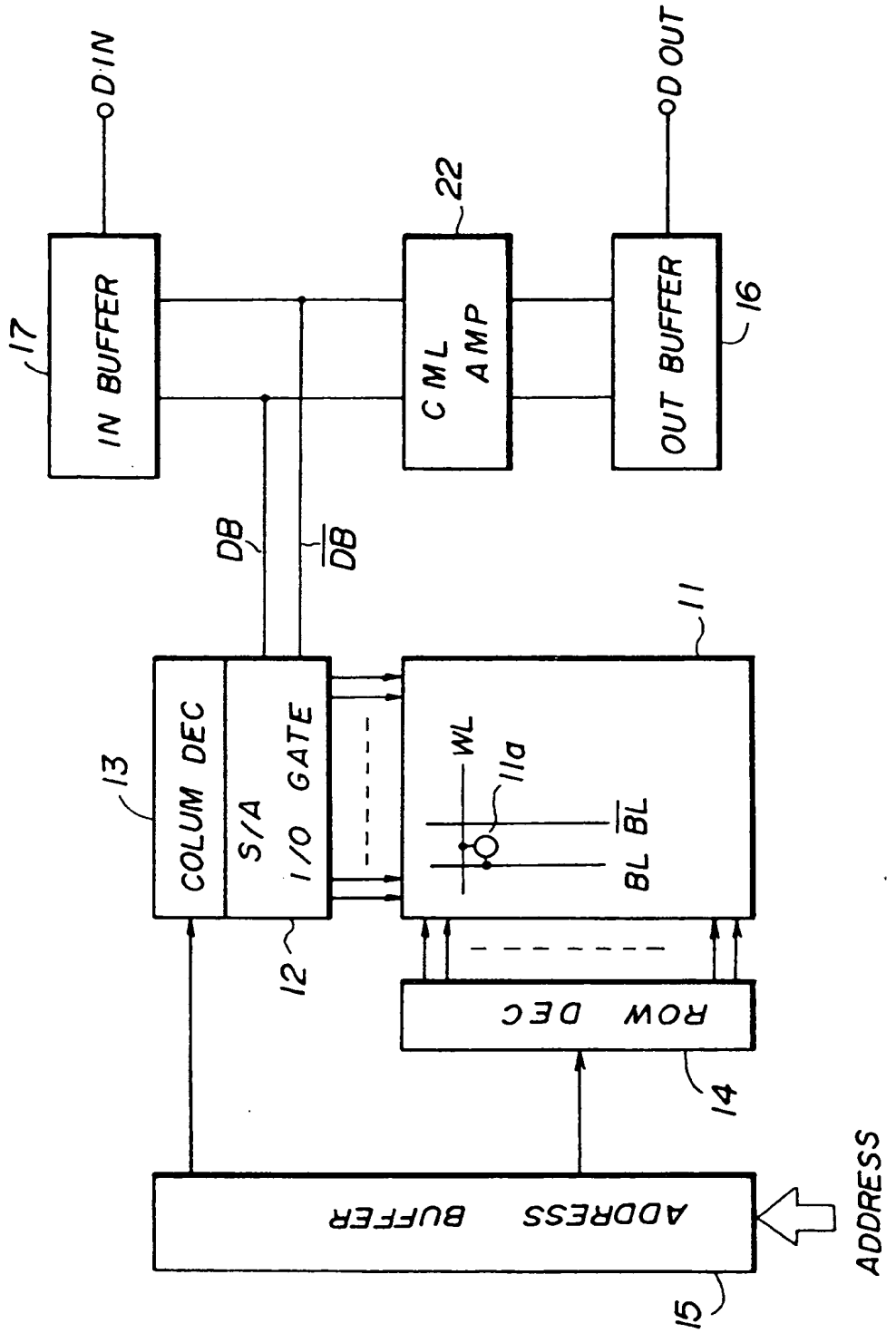
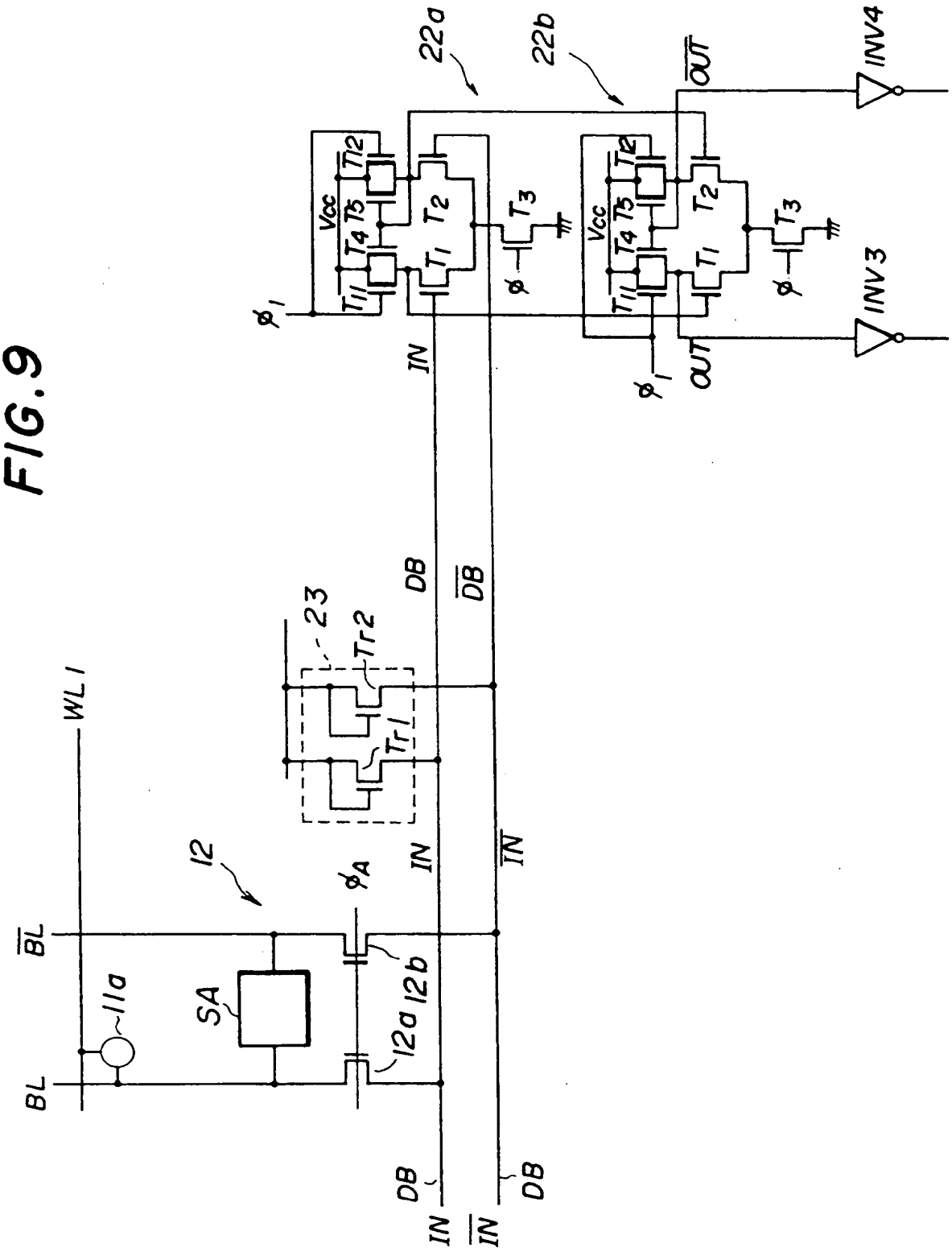


FIG.9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BL
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12a
12b
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IN
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22b
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T5
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T2
T3
φ
OUT
INV4
INV3

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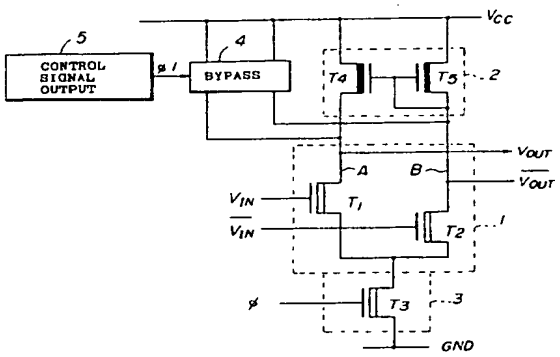
(54) **Current mirror amplifier circuit and method of driving the same.**

(57) A current mirror amplifier circuit includes a differential amplifier circuit (1) having first and second nodes (A, B) for differentially amplifying a pair of complementary input signals in an activation mode, a current mirror circuit (2) coupled between a first power source (Vcc) and the first and second nodes of the differential amplifier circuit, a switching circuit (3) coupled between the differential amplifier circuit and a second power source (GND) which supplies a second voltage lower than a first voltage supplied by the first power source for switching a mode of the differential amplifier circuit from a standby mode to the activation mode in response to an activation signal, and a circuit (4) coupled between the first power source and the first and second nodes of the differential amplifier circuit for pulling up potentials of the first and second nodes during the standby mode, where this circuit is deactivated after the differential amplifier circuit is switched from the standby mode to the activation mode.

FIG. 3



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EUROPEAN SEARCH REPORT

Application Number

EP 91 11 3786

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-4 697 112 (TAKAYUKI OHTANI ET AL.) * column 3, line 20 - column 4, line 34; figures 4-6 *	1-7,10, 11	H03F3/45 H03F3/72 G11C7/06 G05F3/26
A	PATENT ABSTRACTS OF JAPAN vol. 11, no. 400 (E-569)(2847) 26 December 1987 & JP-A-62 159 905 (MITSUBISHI ELECTRIC CORP) 15 July 1987 * abstract *	1,4-6,10	
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS vol. 25, no. 5, October 1990, NEW YORK, US pages 1063 - 1066; SHINGO AIZAKI ET AL.: 'A 15-ns 4-Mb CMOS SRAM' * page 1064, column 2, line 1 - line 19; figure 6 *	2,3	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5) H03F G11C G05F H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	03 APRIL 1992	WALDORFF U.

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